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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,079	12/11/2003	Howard Hao Chen	YOR920030414US1 (8278-650	8481

46069 7590 11/30/2005

F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,079	CHEN ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-22* is/are allowed.

6)☒ Claim(s) *1-4,8-16,23-28,32 and 33* is/are rejected.

7)☒ Claim(s) *5-7 and 29-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/11/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 12/11/2003. **Claims 1-33** are pending.

Claim Objections

1. **Claims 1, 2, 4, 10, 12-16, 23-24, 26, and 28** are objected to because the recited " unit cell/cells" in the claims needs to be clarified. Whether they are " full-unit cell/cells" or "sub-unit cell/cells" or include both.

2. **Claim 5** is objected to because the recited phrase " defining a size of sub-unit cell having a same layout area as the full-unit cell" in the claim (page 38, ll. 11-12) needs to be clarified. Examiner has understood the recited phrase as "defining sub-unit cell having a same layout area as the full-unit cell".

3. **Claim 17 and 20 – 22 are** objected to because the recited " unit cell/cells" in the claims, on p. 41 (line 19), on p. 42 (lines 3, 6,7, and 10), on p. 43 (line 2, 4,6,11, and 17-18); appears to be an error (see the specification on p. 12, lines 1-15). Examiner has understood the recited phrase as "full-unit cell/cells" instead of "unit cell/cells".

4. **Claims 2-9, 11-16, 18-22, and 24-33** are objected to because they depend on the above objected claims.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 1-4, 8-16, 23- 28, and 32-33** are rejected under 35 U.S.C. 102(b) as being anticipated by **Wong et al. (US Patent No. 5952698).**

7. **Referring to claims 1, 10, and 23**, *Wong et al. disclose a layout method for matching pairs of MOSFEFs (see abstract). In Fig. 4 and in the summary (col. 1, ll. 24 to col. 2, ll. 61), Wong et al. disclose two components of an analog circuit (e.g., differential*

amplifiers, a reference current generator, or a regulator), the fist component, which includes transistors 401 and 402, and the second component, which includes transistors 403 and 404 ("unit cells"), have their electrical characteristic matching (transistors 402 and 403 are a matching pair and transistors 401 and 404 can be used as dummy elements). The transistors ("unit cells") in the two components have the same size and are distributed uniformly/evenly in a single row array. In Fig. 3 and in col. 1, line 66 to col. 2, line 22, Wong et al. disclose the electrical characteristics of PMOSFETs can be defined as a function of MOSFET size.

8. **Referring to claims 2-4, 8-9, 11-16, 24-28, and 32-33,** *Wong et al. further teach a step of determining for matching electrical properties of MOSFET transistors (in Figs. 5-11, col.5, ll. 1 to col. 6, ll. 11), based on the tracking to maintain the mean difference in the threshold voltage (i.e. voltage ratio) (Fig. 8, col. 5, ll. 1-24). In Fig. 10 shows a MOSFET device layout array wherein the matched transistors are uniformly distributed, elements 302, 303, 304, and 305, and dummy transistors, elements 301 and 306, are placed near an outer perimeter of the array (see col. 5, ll. 59 to col. 6, ll. 11). The method taught by Wong et al. can be applied for an analog IC circuits, e.g. differential amplifiers, a reference current generator, or a regulator (Fig. 11, col. 2, ll. 29-33)*

Allowable Subject Matter

9. **Claims 17-22** are allowed.

10. **Claims 5-7 and 29-31** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for Allowance

11. **Claims 5-7 and 29-31** would be allowable and **claims 17-22** are allowed because the prior art of record does not teach or fairly suggest the limitations in:

(Claims 5-7)

wherein dividing at least a first component and a second component of a semiconductor integrated circuit into a plurality of unit cells, comprises:

defining a full-unit cell that includes a plurality of sub-elements, wherein each sub-element is used for forming a component;

defining a size of sub-unit cell having a same layout area as the full-unit cell, wherein at least one or more of the sub-elements are dummy elements; and

determining a number full-unit cells and sub-unit cells to be used for forming the first component and the second component .

(Claims 17-22)

A method for matching electrical characteristics of components of a semiconductor integrated circuit, comprising the steps of:

determining components of a semiconductor integrated circuit whose electrical characteristics are to be matched;

defining a unit cell for the components, wherein the unit cell comprises a plurality of sub-elements and wherein the unit cell has a layout area;

defining a sub-unit cell for the components based on the unit cell, wherein the sub-unit cell has the same number of sub-elements and layout area of the unit cell, wherein one or more of the sub-elements of the sub-unit cell are dummy elements;

forming each component using one of more unit cells or one or more sub-unit cells;

defining an array comprising a plurality of cell lots for receiving unit cells or sub-unit cells;

uniformly distributing all unit cells and sub-unit cells of the components in the array; and

placing a dummy cell in each cell lot of the array not occupied by a unit cell or sub-unit cell.

(Claims 29-31)

wherein the unit cells comprise full-unit cells and sub-unit cells, wherein each full-unit cell comprises a plurality of sub-elements that are used for forming a circuit component, and wherein each sub-unit cell comprises a same number of sub-elements as each full-unit cell, wherein one or more of the sub-elements of each sub-unit cell are dummy elements.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

13. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To Tuyen To
Patent Examiner
AU 2825

Paul Dinh